REMARKS

The Office Action of June 4, 2003 was received and carefully reviewed. Reconsideration and withdrawal of the currently pending rejections are requested for the reasons advanced in detail below.

Filed concurrently herewith is a *Request for a Three Month Extension of Time* which extends the shortened statutory period of response to December 4, 2003. Accordingly, Applicants respectfully submit that this response is being timely filed.

Claims 1-12 and 34-74 were pending prior to the instant amendment. By this amendment, claim 1 is amended, claims 2-12 and 34-74 are canceled herein, and new claims 75-96 are added to recite additional features of the present invention to which Applicants are entitled. Consequently, claims 1 and 75-96 are currently pending in the instant application.

Claim Rejections under 35 U.S.C. § 103(a)

Claims 1-12 and 34-74 stand rejected under 35 U.S.C. 103(a) as being unpatentable over JP 11-154714 issued to Yamazaki et al. in light of U.S. Patent 5,656,845 issued to Akbar, and U.S. Patent 5,471,422 issued to Chang et al. The rejection of claims 2-12 and 34-74 is rendered moot by the cancellation thereof. This rejection is traversed for the reasons advanced below as to claim 1.

In response, Applicant has amended claim 1, cancelled claims 2-12 and 34-74, and added new claims 75-96. Support for the present amendments and newly added claims can be found throughout the specification, but more specifically, at least, on page 25, lines 1-9 and page 26, lines 19-25. It is respectfully contended that the claimed invention as presently amended clearly distinguishes the present invention allowable over the proposed combination of Yamazaki, Akbar, and Chang for at least the following reasons.

The claimed invention is directed generally to nonvolatile memory including, *inter alia*, a memory cell array including a plurality of memory cells being formed in a matrix, at least one of the memory cells including a memory thin film transistor and a switching thin film transistor.

Moreover, the nonvolatile memory in accordance with claim 1 as presently amended comprises:

(1) a memory cell array including a plurality of memory cells being formed in a matrix;

(2) at least one of the memory cells including a memory thin film transistor and a switching thin film transistor,

(3) wherein said memory thin film transistor comprises a first semiconductor active layer over an insulating surface, a first insulating film, a floating gate electrode, a second insulating film, a control gate electrode,

(4) wherein said switching thin film transistor includes a second semiconductor active layer over the insulating surface, a gate insulating film, a gate electrode,

(5) wherein the first semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island,

(6) wherein a first thickness of the first semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer of the switching thin film transistor,

(7) wherein the floating gate electrode comprises one of tantalum and tantalum alloy, and

(8) wherein the second insulating film comprises a thermal oxide film of the floating gate electrode.

Applicant respectfully contends that Yamazaki, either alone or in combination with Akbar and Chang, clearly fails to expressly teach, disclose or inherently suggest each and every claim limitation of the prevent invention as presently amended. For the reasons advanced in the responses of August 14, 2002 and February 28, 2003, Applicants continue to believe that the presently claimed invention is patentably distinct over these cited references, the arguments advanced therein being incorporated herein by reference.

Yamazaki also fails to teach additional features of claim 1 as currently amended herein. In particular, Yamazaki does not teach a nonvolatile memory including a floating gate electrode comprising one of tantalum and tantalum alloy, and a second insulating film comprising a thermal oxide film of the floating gate electrode. As a result, the second insulating film may be tantalum oxide and tantalum alloy oxide. Yamazaki teaches that a chrome membrane, aluminum alloy, tantalum, tungsten, molybdenum, and the silicon membrane which provided electroconductivity may be used as the floating gate electrode.

Thus, Yamazaki makes no suggestion that the floating gate electrode comprises one of tantalum and tantalum alloy and the second insulating film comprises one of tantalum oxide and tantalum alloy oxide. Thus, Yamazaki does not teach each and every feature of claim 1, as amended. Furthermore, the teachings of Yamazaki would not render obvious the novel features of the present invention, particularly a floating gate electrode comprising one of tantalum and tantalum alloy and the second insulating film comprises oxide of the floating gate electrode.

In addition, the Examiner asserts that Akbar teaches to form first and second semiconductor layers in a common semiconductor island to provide memory cells with improved performance and reliability. However, Akbar does not teach or suggest that the floating gate electrode comprises one of tantalum and tantalum alloy and the second insulating film comprises an oxide thereof. Thus, Akbar does not overcome the deficiencies of Yamakazi with respect to claim 1, as amended.

Moreover, while the Examiner asserts that Chang teaches to have at least two adjacent cells which share a common signal line therebetween to overcome the problem of delayed programming times, Chang does not teach or suggest that the floating gate electrode comprises one of tantalum and tantalum alloy and the second insulating film comprises one of tantalum oxide and tantalum alloy oxide. Thus, Chang does not overcome the deficiencies of Yamakazi with respect to claim 1, as amended.

Therefore, since the combination of Yamazaki, Chang, and Akbar does not teach, suggest, or render obvious the novel feature of amended claim 1 to a person of ordinary skill in the art, Applicant respectfully requests that the Examiner withdraw the rejection of claim 1 under 35 U.S.C. § 103(a) and place amended claim 1 in immediate condition for allowance.

Provisional Obviousness-Type Double Patenting Rejections

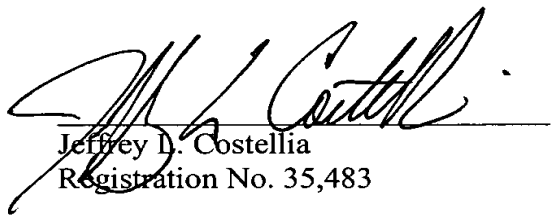
The Examiner provisionally rejects claims 1-12 and 34-74 under the judicially created doctrine of obviousness-type double patenting over claims 1-12 of co-pending U.S. Application No. 09/156,913, in view of Akbar and Yamazaki, and also over claims 1-30 of co-pending U.S. Application No. 09/988,729 in view of Akbar and Yamazaki et al.

However, amended claim 1 contains features which are not taught or suggested by any of U.S. Application No. 09/988,729, Akbar, or Yamazaki. In particular, none of the claims of U.S. Application No. 09/988,729, in combination with Akbar, or Yamazaki, either alone or in combination, teach, suggest, or render obvious to a person of ordinary skill in the art that the floating gate electrode comprises one of tantalum and tantalum alloy and the second insulating film comprises oxide thereof for the reasons stated above. Thus, Applicant respectfully requests that the provisional obviousness-type double patenting rejection be withdrawn and claim 1 be placed in immediate condition for allowance.

New claims 75-96 are also added to recite additional features of the present invention to which Applicants are entitled. Support for the features of these claims is provided above. Consideration and allowance of these claims are respectfully requested.

In view of the foregoing, it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner, that claim 1 be allowed, that new claims 75-96 be allowed and that the application be passed to issue. If a conference would expedite prosecution of the instant application, the Examiner is hereby invited to telephone the undersigned to arrange such a conference.

Respectfully submitted,



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